REMARKS

Claim 2-21 were pending in this application.

Claims 2-5 and 12-15 have been rejected.

Claims 6-11 and 16-19 have been objected to.

Claims 20-21 have been allowed.

Claims 2 and 12 have been amended as shown above.

Claims 2-21 remain pending in this application.

Reconsideration and full allowance of Claims 2-21 are respectfully requested.

I. ALLOWABLE CLAIMS

The Applicant thanks the Examiner for the indication that Claims 20-21 are allowable. Claims 20-21 have not been amended and therefore remain in condition for allowance. The Applicant also thanks the Examiner for the indication that Claims 6-11 and 16-19 would be allowable if rewritten in independent form. Because the Applicant believes that the remaining claims in this application are allowable, the Applicant has not rewritten Claims 6-11 and 16-19 in independent form.

II. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 2-5 and 12-15 under 35 U.S.C. § 102(a) or § 102(b) as being anticipated by U.S. Patent No. 5,475,823 to Amerson et al. ("*Amerson*"). This rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Amerson recites a processor that prevents errors when a compiler advances load instructions in a sequence of instructions. (*Abstract*). The processor stores a load instruction for a particular period of time, which allows the processor to determine if a store instruction to the same address would have been executed before the load instruction. (*Abstract*). If a store instruction would have been executed, the processor uses the same data for the load instruction. (*Abstract*).

First, the Office Action is inconsistent regarding whether or not *Amerson* anticipates all elements of Claims 2 and 12. In making the § 102 rejection, the Office Action asserts that *Amerson* anticipates detecting an instruction without computing "an external memory address of [a] first memory location" as recited in Claims 2 and 12. (*Office Action, Page 3, Paragraph 4*). In making a § 103 rejection, the Office Action later states that *Amerson* does not disclose these elements of Claims 2 and 12. (*Office Action, Page 4, Paragraph 2*).

Second, the Office Action interprets the claims incorrectly. The Office Action interprets Claims 2 and 12 as covering "any method to get the same memory location as long as the address of that location is not calculated during the access level." (*Office Action, Page 2, Paragraph 3*)

(emphasis added). The Applicant notes that Claims 2 and 12 contain no such limitations. In particular, Claims 2 and 12 contain no recitation that an external memory address can be calculated before or after "the access level" but not during "the access level." Claims 2 and 12 are crystal clear – an instruction is detected "without requiring computation of an external memory address." The Office Action is impermissibly reading limitations into Claims 2 and 12.

Third, the Office Action admits that *Amerson* calculates the memory address for a store operation and the memory address for a load operation. (*Office Action, Page 3, Paragraph 4*). The Office Action then admits that *Amerson* compares these two addresses. (*Office Action, Page 3, Paragraph 4*). While the Office Action attempts to draw a distinction between the calculation of the memory addresses and the comparison of the memory addresses in *Amerson*, this distinction does not change the fact that *Amerson* must calculate the memory addresses of both instructions in order to detect a particular instruction. *Amerson* lacks any mention of detecting an instruction "without requiring computation of an external memory address" of a memory location "for the instruction" as recited in Claims 2 and 12.

For these reasons, *Amerson* fails to anticipate the Applicant's invention as recited in Claims 2 and 12 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 102 rejection and full allowance of Claims 2-5 and 12-15.

III. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 2-5 and 12-15 under 35 U.S.C. § 103(a) as being unpatentable over *Amerson* in view of U.S. Patent No. 6,360,314 to Webb, Jr. et al. ("*Webb*").

This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references

when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

As shown in the Applicant's response to the previous Office Action, *Webb* clearly recites that the address of a memory location is calculated and used by the bypass mechanism of *Webb*. (*See, e.g., Col. 6, Lines 6-10*). Once again, the current Office Action attempts to draw a distinction between the calculation of the memory address and the comparisons involving the memory address. However, this distinction cannot change the fact that *Webb* must calculate the memory address of an instruction in order to detect a particular instruction. *Webb* lacks any mention of detecting an instruction "without requiring computation of an external memory address" of a memory location "for the instruction" as recited in Claims 2 and 12.

For these reasons, the proposed *Amerson-Webb* combination fails to disclose, teach, or suggest the Applicant's invention as recited in Claims 2 and 12 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 2-5 and 12-15.

IV. CONCLUSION

As a result of the foregoing, the Applicant asserts that all pending claims in the application are in condition for allowance and respectfully requests an early allowance of such claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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